ABSTRACT OF THE DISCLOSURE

Method and system for testing a sense amplifier in a dynamic memory circuit. In one embodiment, the sense amplifier is connected to a first bit line pair via a first switching device and to a second bit line pair via a second switching device. First memory cells are arranged at crossover points between first word lines and one of the bit lines of the first bit line pair, and second memory cells are arranged at crossover points between second word lines and one of the bit lines of the second bit line pair. Data are written to the first and the second memory cells and subsequently read out. During the read-out of one of the first memory cells, the relevant first word line is activated and the first switching device is activated while the second switching device is closed, and during the read-out of one of the second memory cells, the relevant second word line is activated and the second switching device is activated while the first switching device being closed. One of the first and one of the second memory cells are read in a sequence such that the first and the second switching device are switched multiply during the test of the first and second memory cells.